MAXIMUM DEPOLARIZING VOLTAGE $V_S/2$

WORD LINES AT $V_S/2$

SENSE AMPS BIASED NEAR V_S
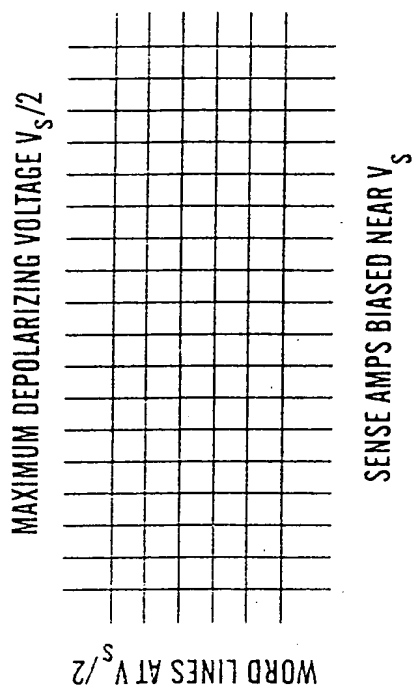
- t_0: WORD LINE LATCHED, ACTIVE PULLDOWN TO 0
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO V_S - SET/RESET GAPS CELL
- t_6: WORD LINE RETURNED TO QUIESCENT $V_S/2$
- t_7: BIT LINES ACTIVELY RETURNED TO V_S CLAMP
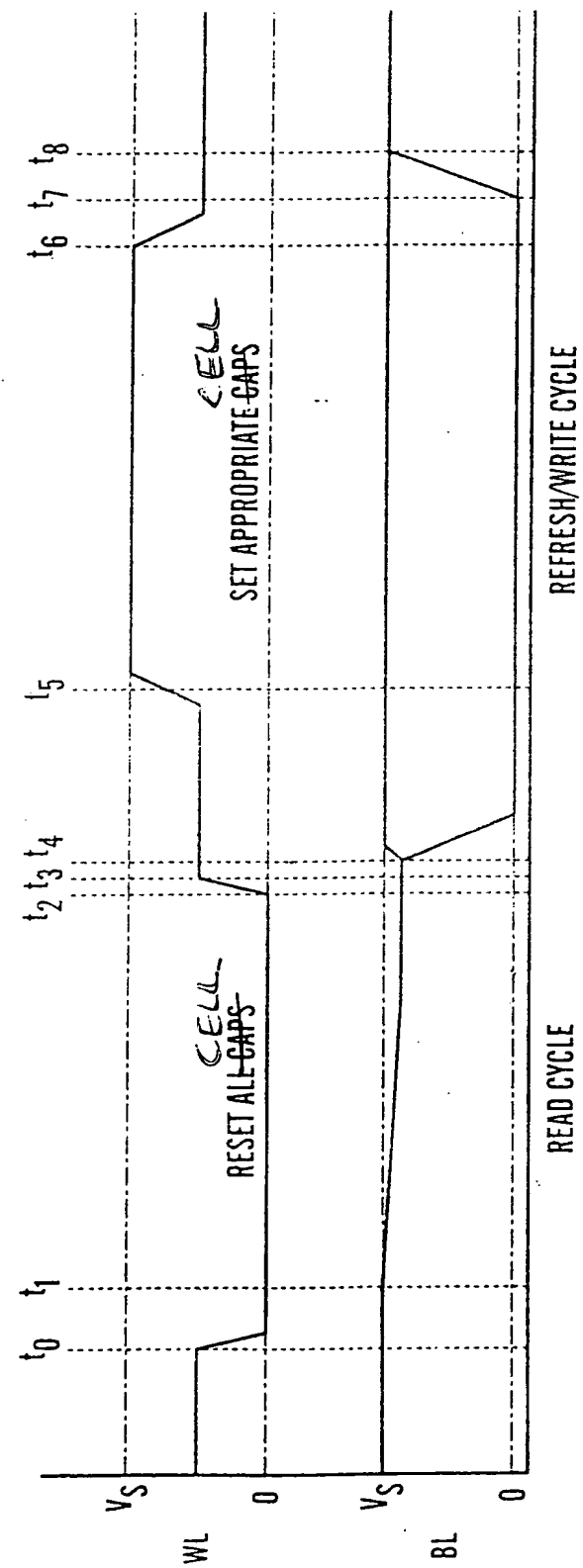- t_8: READ/WRITE CYCLE COMPLETE

CELL
RESET ALL GAPS

CELL
SET APPROPRIATE GAPS

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8

V_S
WL
0

V_S
BL
0

READ CYCLE

REFRESH/WRITE CYCLE

Fig.4

- t_0: WORD LINE LATCHED, ACTIVE PULL UP TO V_s
- t_1: BIT LINE CLAMP RELEASED - SENSE AMP ON
- t_2: BIT LINE DECISION - DATA LATCHED
- t_3: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_4: WRITE DATA LATCHED ON BIT LINES
- t_5: WORD LINE PULLED TO 0 - SET/RESET CAPS *CELL*
- t_6: WORD LINE RETURNED TO QUIESCENT $V_s/2$
- t_7: BIT LINES ACTIVELY RETURNED TO 0 CLAMP
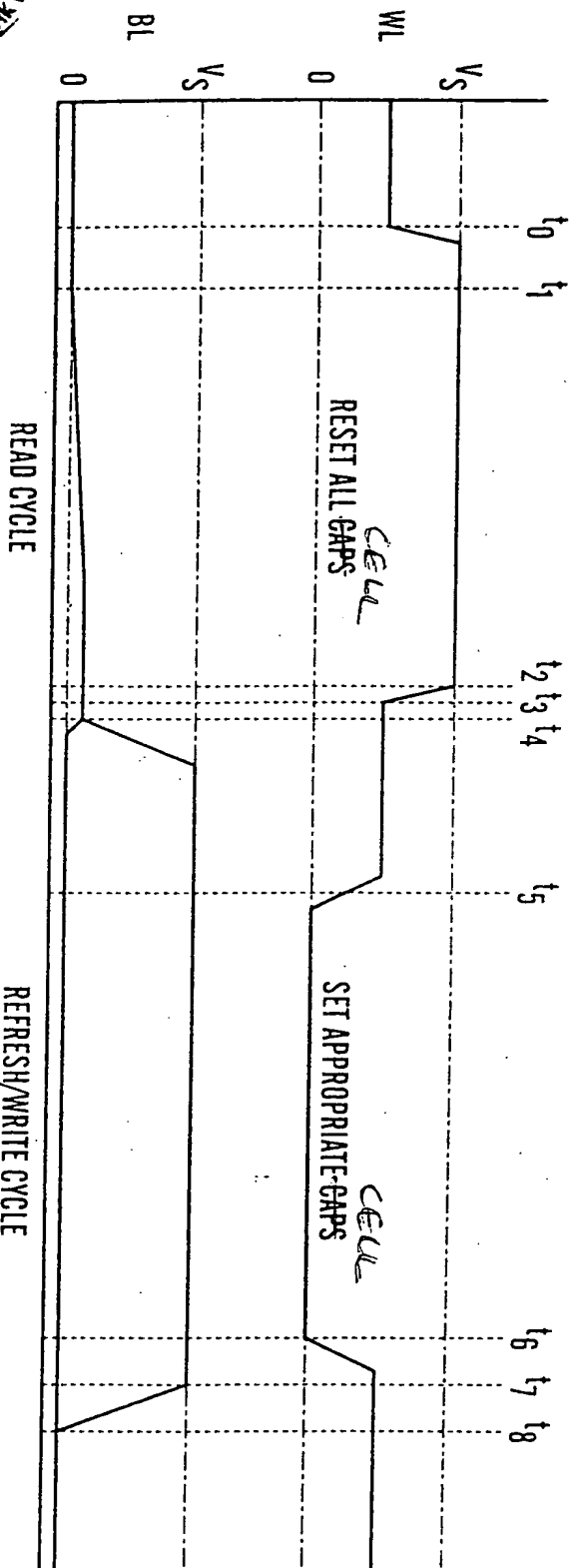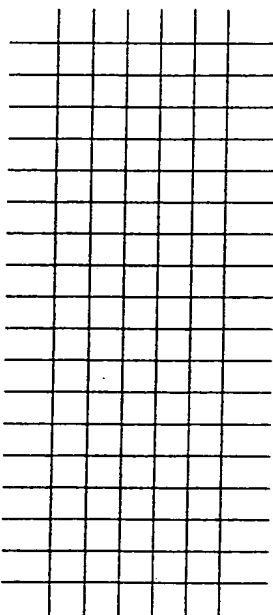- t_8: READ/WRITE CYCLE COMPLETE

WL

BL

V_s

0

V_s

0

V_s

0

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8

RESET ALL CAPS *CELL*

SET APPROPRIATE CAPS *CELL*

READ CYCLE

REFRESH/WRITE CYCLE

Fig.5

WORD LINES AT $V_s/2$

MAXIMUM DEPOLARIZING VOLTAGE $V_s/2$

SENSE AMPS BIASED NEAR V_s